

## ABSTRACT

In a high speed memory subsystem differences in each memory  
5 device's minimum device read latency and differences in signal propagation  
time between the memory device and the memory controller can result in  
widely varying system read latencies. The present invention equalizes the  
system read latencies of every memory device in a high speed memory system  
by comparing the differences in system read latencies of each device and then  
10 operating each memory device with a device system read latency which causes  
every device to exhibit the same system read latency.